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09/917,127	07/27/2001	Larry D. Kinsman	3572.1US (97-1243.1)	3326

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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/917,127	Applicant(s) KINSMAN ET AL.	
	Examiner Michael Trinh	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *February 12, 03 and Oct 21, 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6 and 10-29* is/are pending in the application.

4a) Of the above claim(s) *19,20 and 25-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,10-18 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed on October 21, 2003 and Election filed on February 12, 2003. Claims 5 and 7-9 were canceled. Claims 1-4, 6, and 10-29 are currently pending, in which claims 19-20,25, and 26-29 are non-elected without traverse.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Election/Restrictions

1. Election filed 2/12/03 was made without traverse as treated in Paper No. 11. Since claim 25 is directed to subject matter of placing the semiconductor substrate having a plurality of individual die locations in aligning with terminal pads of a carrier substrate, as similarly recited in claim 19. Claim 25 is regrouped into Group II including claims 19-20 as non-elected invention, and constructively withdrawn from consideration.

Accordingly, claims 19-20, 25, and 26-29 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, without traverse, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 103

2. Claims 1-3,6,10-14,17, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi (6,107,164) taken with Chakravorty (6,181,569).

Ohuchi teaches a method for forming a semiconductor device comprising at least the steps of: providing a semiconductor substrate 10 having an active surface including at least a layer 2 of integrated circuit, with a plurality of die, with plurality of bond pads 3 with each die; forming intermediate conductive elements 4 (Fig 1; cols 3A-3D) over the bond pads to project a height over the active surface; forming a pattern of mutually traverse channels 22 to depth below the layer and circumscribing a die and exposing peripheral edges of the circuit device (Fig 3B; col 3, lines 9-45), wherein the channels have parallel sidewalls (re claim 6); applying an encapsulant material 23 (Fig 3C) over the channels and dies to a depth exceeding the height of the projection; removing the encapsulant material 23 by abrasive polishing planarization to expose the conductive elements (Fig 3D; col 3, line 30 through col 4, re claim 10); and forming an external conductive elements 5 over the intermediate conductive elements 4 (Figs 4; re claim

2). Re claims 3 and 23, the method further comprises severing the substrate in alignment with the channels into a plurality of semiconductor elements, each element comprised of at least one individual die location, wherein the exposed peripheral edges of the integrated circuitry remain covered with the encapsulant material 23 (Fig 4c; col 3, line 45 through col 4). Re claim 12, wherein the conductive elements 4 comprises pillars of conductive copper (col 2, lines 60-63). Re claim 14, wherein external conductive elements comprises solder balls (col 3, lines 43-45). Re claim 17, wherein the encapsulant material is resin (col 3, lines 25-35).

Re claim 1, Ohuchi applies an encapsulant material, but lacks to mention by transfer molding.

However, Chakravorty teaches (at col 9, lines 65-67; col 9, lines 55 through col 10, line 65; Figs 8B-8C) applying an encapsulant material 312 over the active surface of a substrate exceeding the height of projection of the intermediate conductive elements 311 by employing several alternative techniques such as transfer molding by using epoxy resin based mold compound, laminating with a dry film, or coating from a liquid solution, wherein forming the encapsulant material over the substrate by transfer molding would conformally seal and encapsulate the substrate with a resin.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply an encapsulant material on the substrate wafer of Ohuchi by known transferring molding method as taught by Chakravorty, because the transferring molding method would conformally seal the substrate wafer with a resin, wherein all integrated circuit dice in the wafer are encapsulated with the encapsulant material at the same time.

Re further claims 11 and 13, Ohuchi forms the intermediate conductive elements 4 of pillar posts, but lacks mentioning forming the conductive elements as solder ball by wire bonding. However, Chakravorty teaches (at col 8, line 57 through col 9; col 13, lines 35-62;) several alternative processes for forming on the bond pad the intermediate conductive elements (311,322,323, 325,326 in Figs 5a,6,8d,10c-g) having the shape of pillar bump and solder balls, wherein wire bonding capillary is used for forming the conductive elements (col 9, liens 10-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive elements of Ohuchi by employing several established techniques including wire bonding capillary for solder balls as taught by Chakravorty, because

these established techniques are alternative and art recognized equivalent for forming a conductive elements on the bond pads, wherein different shapes of the conductive elements depend on the process of their formation.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi (6,107,164) taken with Chakravorty (6,181,569), as applied to claims 1-3,6,10-14,17, and 23 and further of Abe et al (4,610,079).

Ohuchi and Chakravorty teach a method for forming a semiconductor device as applied to claims 1-3,6,10-14, 17, and 23 above.

Ohuchi shows the channels having U-shape with parallel sidewalls, as similarly recited in claim 6, while claim 4 alternatively recites the channels having sloped sidewalls.

Abe teaches forming in the wafer dicing lines of either U-shaped channel having parallel sidewalls (Fig 2a) or V-shaped channel having sloped sidewalls (Fig 2b; col 2, lines 19-54).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the channels of Ohuchi to have a U-shape or V-shape as taught by Abe, because channels of either shape facilitate easy dicing and breaking of the wafer into a plurality of individual dies, wherein these channels are art recognized equivalent and alternative for substitution as scribe lines.

4. Claims 18,21-22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi (6,107,164) Chakravorty (6,181,569), as applied above to claims 1-3,6,10-14,17, and 23, and further of Brooks et al (5,824,569) and Heo (5,908,317).

Ohuchi and Chakravorty teach a method for forming a semiconductor device as applied to claims 1-3,6,10-14, 17 and 23 above. Re claim 22, Ohuchi teaches (at Fig 6; col 6, lines 2-12) forming a bond pad 13 on exposed portions of the intermediate conductive elements 4.

Re claims 21,24, and 25, Ohuchi lacks flip-chip bonding the semiconductor element to a carrier substrate having conductive bumps as terminal pads. Re claim 18, forming encapsulant material in the back of the substrate.

However, Brooks '569 teaches (at Fig 6) flip-chip bonding and aligning the semiconductor element having the conductive elements 32 to conductive terminals inherently

formed on a carrier substrate PC board 50. Re claim 18, Brooks also teaches (at Figs 3-5) forming an encapsulant material 36A in the back of the substrate 30. Heo teaches (at figs 7A-8; column 7) aligning conductive elements 20 to conductive bumps as terminal pads formed on a carrier substrate 40 (Fig 7A).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to align the conductive elements of the semiconductor device of Ohuchi to conductive bumps formed on a carrier substrate as taught by Brooks and Heo. This is because of the desirability to package the chip on a PC board by flip chip techniques. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the method of Ohuchi by also encapsulating the back side of the substrate with an encapsulant material as taught by Brooks, because it would protect the back side of the substrate from contamination and damage.

5. Claim 17 is further rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi (6,107,164) and Chakravorty (6,181,569), as applied above to claims 1-3,6,10-14,17, and 23, and further of Farnworth (5,933,713).

Ohuchi and Chakravorty teach a method for forming a semiconductor device as applied to claims 1-3,6,10-14, 17 and 23 above.

Ohuchi teaches resin for the encapsulant material (col 3, lines 25-35), but lacks mentioning other encapsulant materials as recited in claim 17.

However, Chakravorty teaches (at col 9, line 60 through col 10, line 7) employing the encapsulant materials of epoxy resin, polyimides, polymeric, etc.. Farnworth '713 teaches (at Fig 5; col 6, lines 16-41) encapsulating the substrate with an encapsulant materials including polymers, epoxies, silicones, silicone-carbon resins, polyimides, polyurethanes, and glasses.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to encapsulate the substrate of Ohuchi by using other alternative encapsulant materials including polymers, epoxies, silicones, silicone-carbon resins, polyimides, polyurethanes, and glasses, as further taught by Chakravorty and Farnworth '713. This is because of the desirability to encapsulate and protect the substrate, wherein these encapsulant materials are art recognized equivalent and alternative for substitution in encapsulating the wafer.

6. Claims 12 and 15 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi (6,107,164) and Chakravorty (6,181,569), as applied above to claims 1-3,6,10-14,17, and 23, and further of Farnworth (5,933,713) and Farnworth (6,020,629).

Ohuchi and Chakravorty teach a method for forming a semiconductor device as applied to claims 1-3,6,10-14, 17 and 23 above.

Ohuchi already teaches forming the conductive elements of conductive pillar post and solder balls while claims 12 and 15 further recites alternative materials for conductive elements including conductor filled epoxy, or a metal filled elastomer.

However, Ohuchi teaches the conductive elements 4 comprising pillars of conductive copper (col 2, lines 60-63). Chakravorty teaches (at col 8, line 57 through col 9; col 13, lines 35-62;) several alternative processes for forming the conductive elements (311,322,323, 325,326 in Figs 5a,6,8d,10c-g) having the shape of pillar bump and solder balls, wherein different shapes of the conductive elements depend on the process of their formation. Farnworth '713 teaches (at col 8, lines 35-67; Figs 12-15) forming the conductive elements 70 by applying a conductive elastomer material such as a metalized rubber instead of solder balls 30 as shown in Figure 2, col 5, lines 38-65. Farnworth '629 teaches (at col 5, lines 1-11) forming a conductive elements by using metal, or conductive elastomer, such as epoxy or silicone with embedded metal particles.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive elements of Ohuchi by employing pillars of conductive metal, conductor-filled epoxy, or metal filled elastomer, as combinatively taught by Ohuchi, Chakravorty, Farnworth '629, and Farnworth '713. This is because of the desirability to form the conductive elements for electrical connection, wherein these conductive materials are art recognized equivalent and alternative for substitution in forming conductive elements for electrical connection.

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi (6,107,164) and Chakravorty (6,181,569), as applied above to claims 1-3,6,10-14,17, and 23, and further of Yew et al (6,137,164).

Ohuchi and Chakravorty teach a method for forming a semiconductor device as applied to claims 1-3,6,10-14, 17 and 23 above.

Ohuchi already teaches forming the external conductive elements 5 of solder balls over the intermediate conductive elements 4 while claim 16 recites alternative technique for forming the external conductive elements by applying an anisotropically conductive film.

However, Yew teaches (at Figs 6A-6B; col 7, lines 4-38) an alternative technique for forming the external conductive elements by applying an anisotropic conductive film, wherein compression causes formation of the external conductive elements for electrically contacting between the two circuits.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the external conductive elements of Ohuchi by applying an anisotropic conductive film as taught by Yew et al. This is because of the desirability to form the external conductive elements for electrical connection between two circuits, wherein these alternative techniques art recognized equivalent and alternative for substitution in forming conductive elements for electrical connection.

Response to Arguments

8. 35 USC 102 rejection: Applicant's amendment of claim 1 to further recite the limitation of"...transfer molding..." have overcome the 35 USC 102 rejection using Ohuchi reference in the last office action, since Ohuchi 6,107,164 does not anticipatively disclose the limitation.

9. 35 USC 103 rejection: Applicant's remarks filed October 21, 2002 have been fully considered but they are not persuasive and in moot of new ground of rejections.

** Applicant's remarks (at remark filed 10/21/03) that "...Ohuchi does not disclose limitation" of"transfer molding...".

In response, this is noted and found unconvincing. Under 35 USC 103 rejection, although Ohuchi does not disclose limitation" of"transfer molding, forming the encapsulant material over the substrate by transfer molding, as well-known, would have been obvious to one of ordinary skill in the art because of the desirability to conformally sealing the substrate with a resin. Moreover, at least Chakravorty evidently teaches (at col 9, lines 65-67; col 9, lines 55

through col 10, line 65; Figs 8B-8C) applying an encapsulant material 312 over the active surface exceeding the height of projection of the intermediate conductive elements 311 by employing several alternative techniques such as transfer molding by using epoxy resin based mold compound, laminating with a dry film, or coating from a liquid solution. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply an encapsulant material on the substrate wafer of Ohuchi by known transferring molding method as evidently taught by Chakravorty, because the transferring molding method would conformally seal the substrate wafer with a resin, wherein all integrated circuit dice in the wafer are encapsulated with the encapsulant material at the same time.

Secondary references are cited to evidently show well known limitations, alternative materials and techniques for forming the semiconductor devices. Accordingly, the rejections clearly established a prima facie case of obviousness.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs

Michael Trinh
Primary Examiner